

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Claims 1-18 (Cancelled)

1 19. (Original) A memory apparatus comprising:
2 a first memory chip;
3 a second memory chip; and
4 a designated terminal to be supplied an operation
5 voltage,
6 wherein said first memory chip has a first terminal, a
7 second terminal and a voltage circuit,
8 wherein said second memory chip has a third terminal,
9 wherein said designated terminal couples to said first
10 terminal of said first memory chip and said third terminal
11 of said second memory chip and is supplied an operation
12 voltage,
13 wherein said second terminal of said first memory chip
14 is supplied one of a first state signal and a second state
15 signal according to a voltage level of said operation
16 voltage,

17 wherein said second terminal is supplied said first
18 state signal, said first memory chip is supplied a first
19 voltage as said operation voltage and generates an internal
20 operation voltage from said first voltage by said voltage
21 circuit,

22 wherein said second terminal is supplied said second
23 state signal, said first memory chip is supplied a second
24 voltage as said operation voltage and generates said
25 internal operation voltage from said second voltage by said
26 voltage circuit, and

27 wherein said first voltage is lower voltage than said
28 second voltage.

1 20. (Original) A memory apparatus according to claim
2 19,

3 wherein said voltage circuit comprises a charge pump
4 including a plurality of stages,

5 wherein when said second terminal is supplied said
6 first state signal, said voltage circuit uses a first stage
7 of said charge pump,

8 wherein when said second terminal is supplied said
9 second state signal, said voltage circuit uses a second
10 stage of said charge pump, and

11 wherein a boost rate of said first stage is more than
12 a boost rate of said second stage.

1 21. (Original) A memory apparatus according to claim
2 20, further comprising a fourth terminal,
3 wherein said fourth terminal is supplied a reference
4 voltage,

5 wherein said second terminal is fixedly coupled to one
6 of said operation voltage or said reference voltage as said
7 first state signal, and

8 wherein said second terminal is fixedly coupled to
9 another one of said operation voltage or said reference
10 voltage as said second state signal.

1 22. (Original) A memory apparatus according to claim
2 21,
3 wherein said reference voltage is a ground level.

1 23. (Original) A memory apparatus according to claim
2 22,
3 wherein said first memory chip is a volatile memory,
4 and
5 wherein said second memory chip is a nonvolatile
6 memory.

1 24. (Original) A nonvolatile memory apparatus
2 comprising:
3 a first semiconductor chip;
4 a nonvolatile memory chip; and
5 a designated terminal pair for being supplied an
6 operation voltage,
7 wherein said first semiconductor chip has a first
8 terminal pair coupled to said designated terminal pair,
9 wherein said nonvolatile memory chip has a voltage
10 circuit, a second terminal pair coupled to said designated
11 terminal pair and a third terminal for being supplied one
12 of a first state signal and a second state signal according
13 to a voltage level of said operation voltage,
14 wherein when said third terminal is supplied said
15 first state signal, said nonvolatile memory chip is

16 supplied a first voltage as said operation voltage and
17 generates an internal operation voltage from said first
18 voltage by said voltage circuit,
19 wherein when said third terminal is supplied said
20 second state signal, said nonvolatile memory chip is
21 supplied a second voltage as said operation voltage and
22 generates said internal operation voltage from said second
23 voltage by said voltage circuit and,
24 wherein said first voltage is lower than said second
25 voltage.

1 25. (Original) A nonvolatile memory apparatus
2 according to claim 24,
3 wherein said nonvolatile memory has a nonvolatile
4 memory array, and wherein said voltage circuit generates a
5 program voltage for programming data to said nonvolatile
6 memory array.

1 26. (Original) A nonvolatile memory apparatus
2 according to claim 25,
3 wherein said voltage circuit further generates an
4 erase voltage for erasing data stored in said nonvolatile
5 memory array.

1 27. (Original) A nonvolatile memory apparatus
2 according to claim 26,
3 wherein when said first semiconductor chip is only
4 operable by said second voltage as said operation voltage,
5 and said third terminal of said nonvolatile memory is
6 fixedly supplied said second state signal.